Wide Vin 50V Non-synchronous Boost/Flyback/SEPIC Controller

FEATURES

- Qualified for Automotive Applications
- Wide Input Voltage Range: 3.2V-50V
- Low Shutdown Current 3.7uA
- Low Quiescent operating Current: 450uA
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- Integrated Frequency Dithering for EMI Mitigation
- External Frequency Synchronic
- External Compensation
- Supports additional Slope Compensation
- 22ms Internal Soft-start Time
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjust Under-Voltage Lockout
  - Optional Hiccup Over Load Protection
  - Thermal Shutdown Protection:165°C
- MSOP-8L(3mm*3mm) Package

APPLICATIONS

- Muti-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application

DESCRIPTION

The SCT81620 device is a wide input, non-synchronous boost controller. The Device can be used in Boost, SEPIC and Flyback converters and topologies.

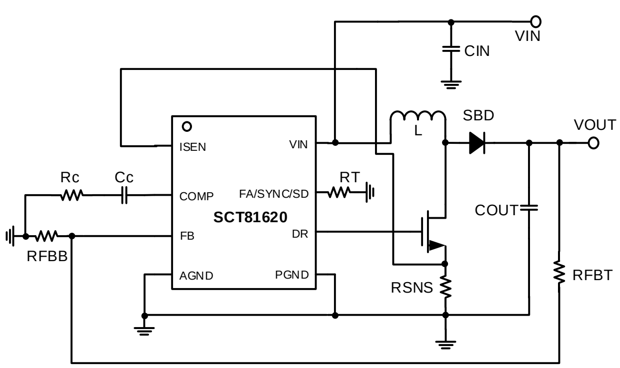
The switching frequency of the SCT81620 device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is adjustable through an external resistor.

The SCT81620 is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81620 features Frequency Spread Spectrum (FSS) with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

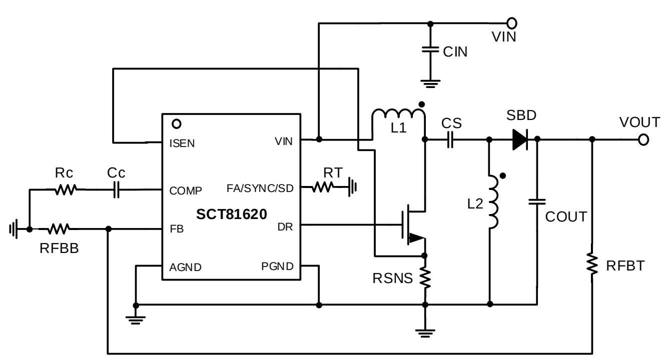
The SCT81620 device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 3.7 µA. Integrated current slope compensation simplifies the design and, if needed for specific applications, can be increased using a single resistor.

The device is available in a MSOP-8L(3mm*3mm) Package.

TYPICAL APPLICATION



BOOST



SEPIC

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Update Device Order Information

DEVICE ORDER INFORMATION

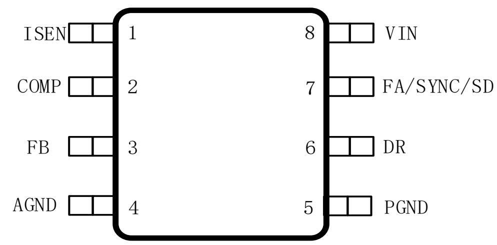
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT81620MTDR	Tape & Reel	4000	1620	8	8-Lead 3mm×3mm Plastic MSOP

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	62	V
DR	-1	6.6	V
ISEN, COMP, FB, FA/SYNC/SD	-5	5.5	V
Peak Driver Output Current		1(2)	A
Junction temperature(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 8-Lead Plastic MSOP 3mmx3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Guaranteed by design, not tested in productions.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	DESCRIPTION
ISEN	1	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
COMP	2	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and GND.
FB	3	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage. The device regulates FB voltage to the internal reference value of 1.26V typical.
AGND	4	Analog ground pin.
PGND	5	Power ground pin.
DR	6	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
FA/SYNC/SD	7	Switching frequency setting pin. The switching frequency is programmed by a single resistor between this pin and AGND. The internal clock can be synchronized to an external clock. A high level on this pin for ≥ 30 μs will turn the device off and the device will then draw 3.7 μA from the supply typically.
VIN	8	Power supply input pin

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.2	50	V
V_{CC}	VCC voltage range	3.2	6.1	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	MSOP-8	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	132.8	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	64.1	°C/W
$R_{\theta JB}$	Junction to board thermal resistance(1)	83.8	°C/W

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81620 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81620. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.92		50	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.9 160		V mV
I_{SD}	Shutdown current	$V_{FA/SYCN/SD}$=5V		3.7	8	uA
I_Q	Quiescent current from VIN	no load, no switching		460		uA
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	1.241	1.26	1.278	V
		Tj=-40~125°C	1.222		1.297	
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V	500	700	900	uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V	120	155	195	uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V	-170	-130	-90	uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V	1.9	2.55	3.2	V
V_{COMP_L}	COMP low clamp	V_{FB}=1.7V	0.4	0.88	1.2	V
Gate Driver						
R_{DSON_TOP}	Driver switch on resistance(top)			4		Ω
R_{DSON_LOW}	Driver switch on resistance(bottom)			2		Ω
Current Sense						
Vsense	Current sense threshold		120	146	170	mV
V_{SL}(2)	Internal compensation Ramp voltage			90		mV
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated (SS_done)		64		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS release		32768		cycles
Soft start						
T_{SS}	Soft-start Time			22		ms
Switching Frequency						
F_{SW}	Switching frequency	$R_{FA/SYNC/SD}$=47.5kΩ	360	400	440	kHz
F_{SS}	Frequency Spread Range			6		%
V_{SYN_HI}	Threshold for Synchronization on FA/SYNC/SD pin	Synchronization voltage rising		1.27	1.45	V
V_{SYN_LO}		Synchronization voltage falling	0.58	0.68		V
D_{MAX}	Maximum Duty Cycle	$R_{FA/SYNC/SD}$=47.5kΩ	85	91		%

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON_MIN}	Minimum on-time	Fsw=400kHz		250		ns
Protection						
V_{OVTH}(3)	FB overvoltage threshold	FB rising	25	85	135	mV
		Hysteresis	30	80	130	mV
T_{SD}(1)	Thermal shutdown threshold	T_J rising		165		°C
	Hysteresis			25		°C

(1) Guaranteed by design and bench, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) The overvoltage protection is specified with respect to the feedback voltage. This is because the overvoltage protection tracks the feedback voltage. The overvoltage threshold can be calculated by adding the feedback voltage (V_{FB}) to the overvoltage protection specification.

TYPICAL CHARACTERISTICS

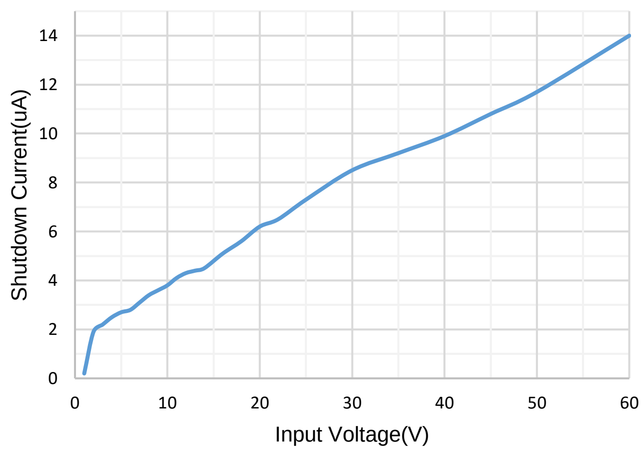


Figure 1. ISD vs Input Voltage

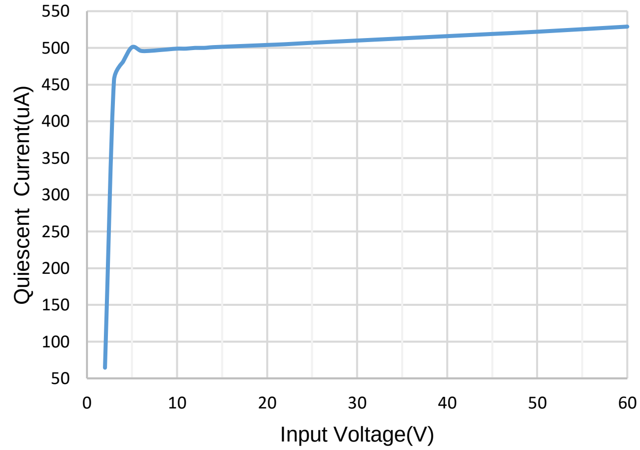


Figure 2. IQ vs Input Voltage

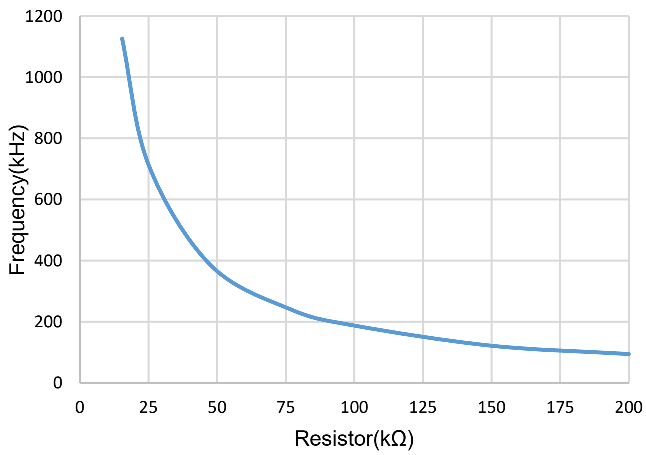


Figure 3. Switching Frequency vs RT

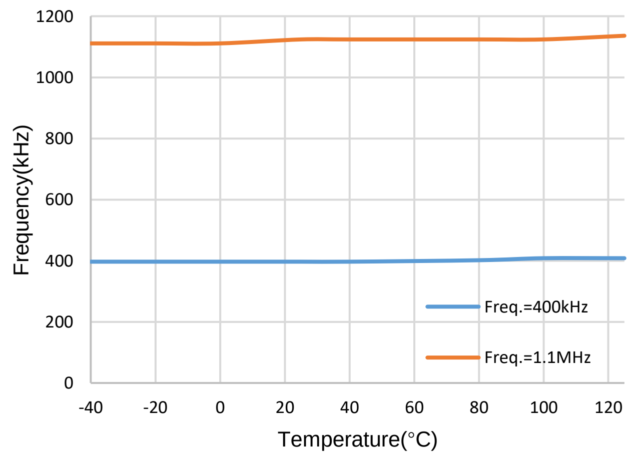


Figure 4. Switching Frequency vs Temperature

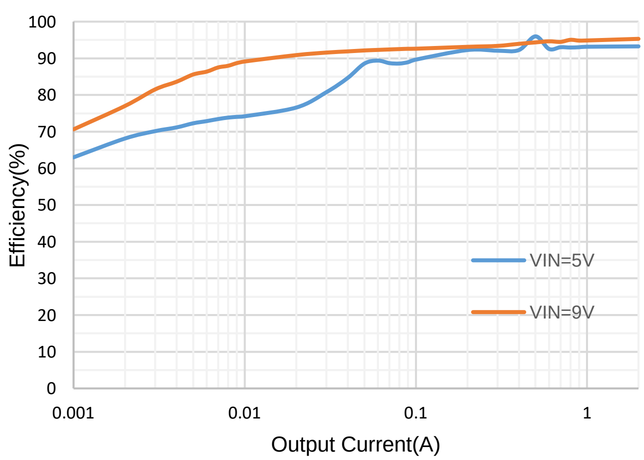


Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

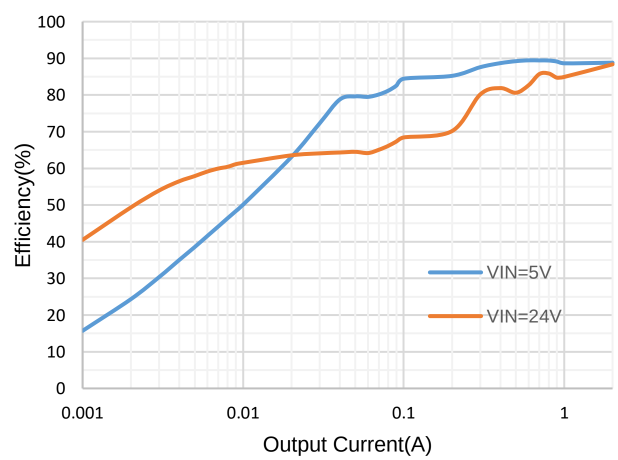


Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

TYPICAL CHARACTERISTICS

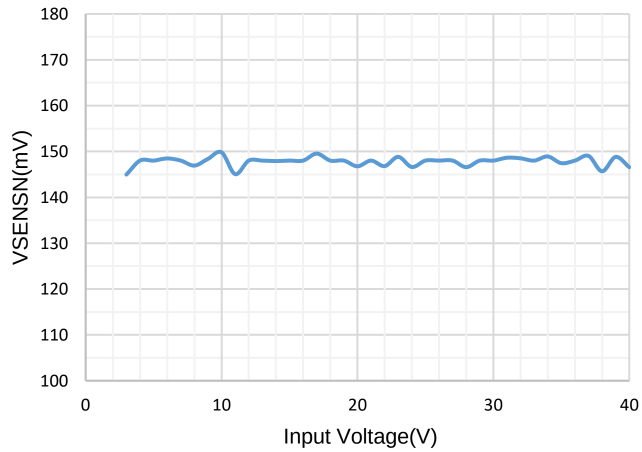


Figure 7. VSENSN vs Input Voltage

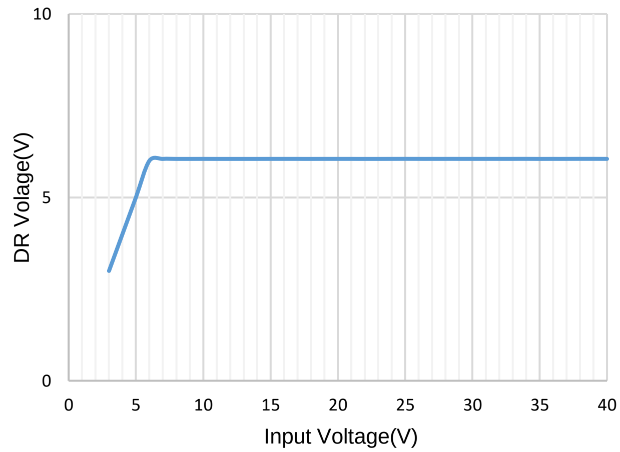


Figure 8. DR Volage vs Input Voltage

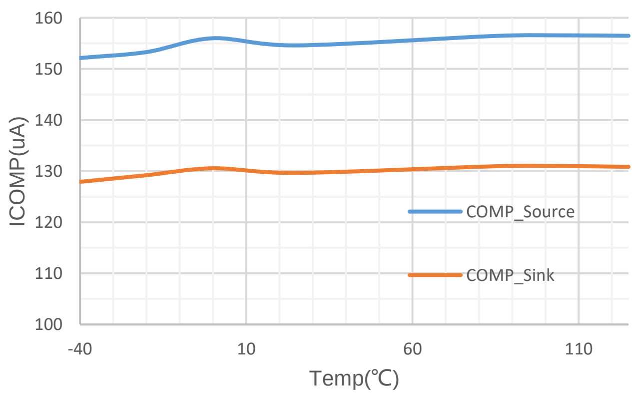


Figure 9. COMP Current vs Temperature

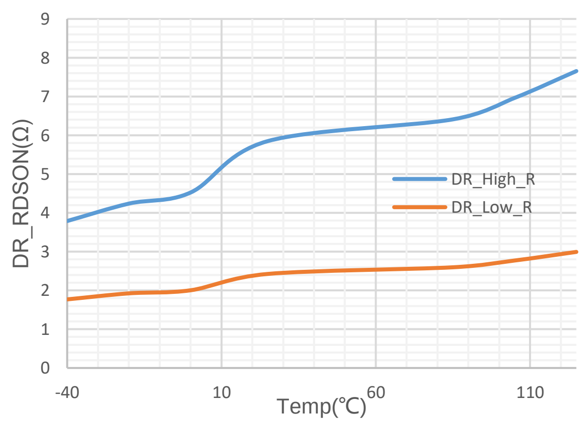


Figure 10. DR Resistance vs Temperature

FUNCTIONAL BLOCK DIAGRAM

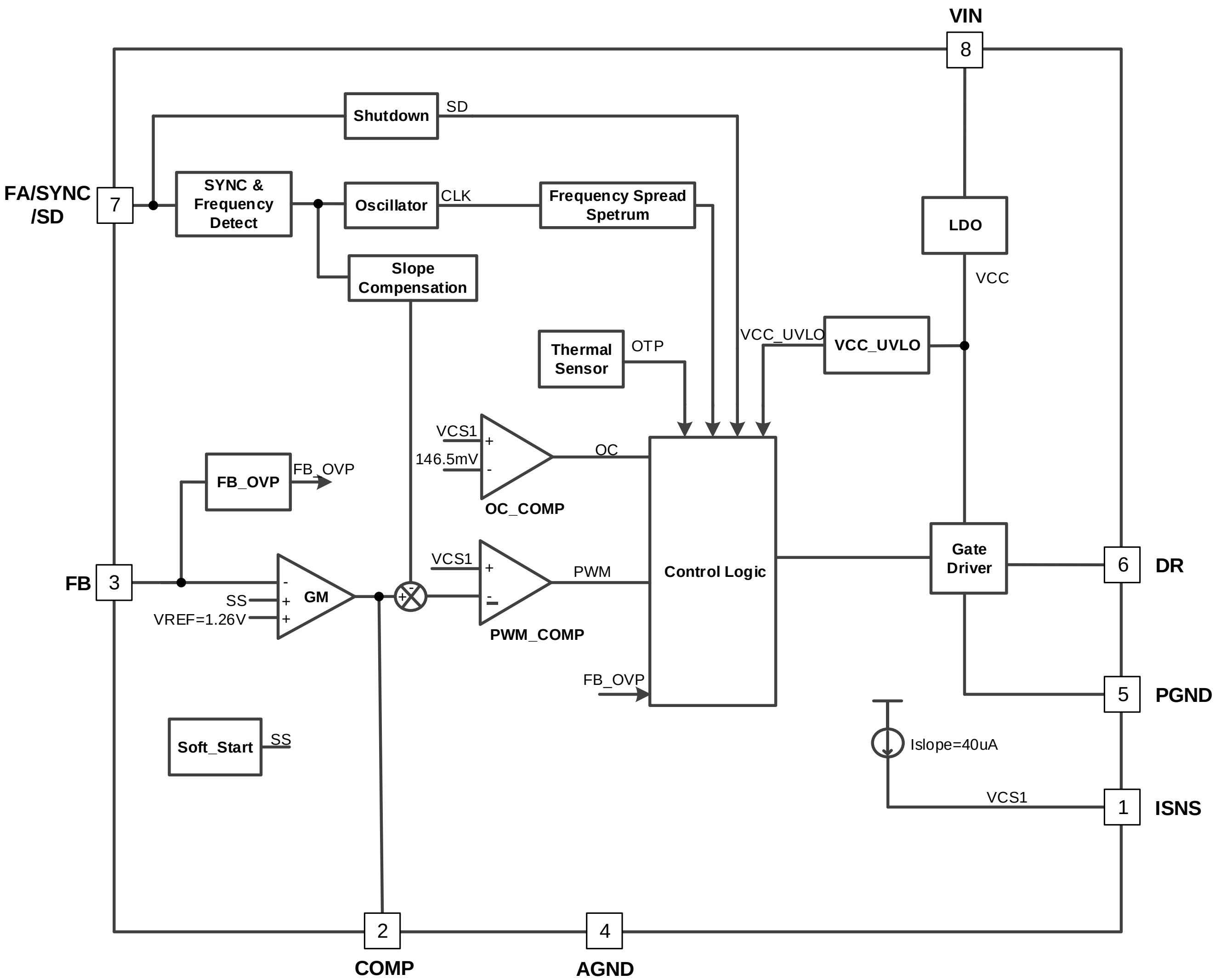


Figure 11. Functional Block Diagram

OPERATION

Overview

The SCT81620 device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the ISNS pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off. The voltage sensed across the sense resistor generally contains spurious noise spikes, these spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET in on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the SCT81620 prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

The SCT81620 works at Pulse skip mode to further increase the efficiency in light load condition. The quiescent current of SCT81620 is 450uA typical under no-load condition and not switching. Disabling the device, the typical supply shutdown current on VIN pin is 3.7μA.

Overvoltage Protection

The SCT81620 has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at any time the voltage at the feedback pin rises to 1.345V (typ.), OVP is triggered. OVP will cause the DR pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The SCT81620 begins switching again when the feedback voltage reaches 1.265V (typ.).

Slope Compensation Ramp

The SCT81620 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. However, current mode control has a Sub-harmonic Oscillation when duty cycles greater than 50%. To prevent the Sub-harmonic oscillations, a compensation ramp is added to the control signal.

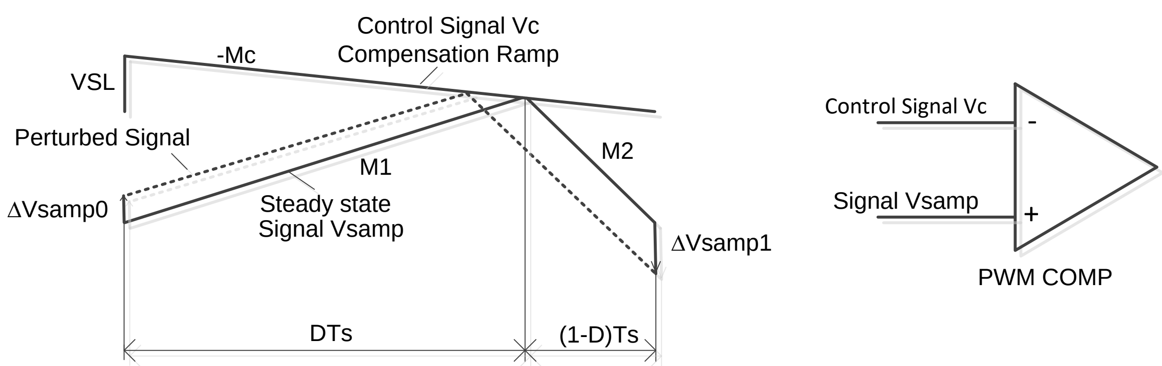


Figure12. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

The current mode control scheme samples the inductor current, IL, and compares the sampled signal, Vsamp, to a internally generated control signal, Vc. The current sense resistor, RSEN, as shown in Figure11 converts the sampled inductor current, IL, to the voltage signal, Vsamp, that is proportional to IL such that：

$$V_{samp} = I_L * R_{SEN} \tag{1}$$

Figure12 illustrate the theory why Sub-Harmonic Oscillation happen, the rising and falling slopes, M1 and -M2 respectively, of Vsamp are also proportional to the inductor current rising and falling slopes, Mon and -Moff respectively. Where Mon is the inductor slope during the switch on-time and -Moff is the inductor slope during the switch off-time and are related to M1 and -M2 by：

$$M_1 = M_{on} * R_{SEN} \tag{2}$$

$$-M_2 = -M_{off} * R_{SEN} \tag{3}$$

For the boost topology:

$$M_1 = M_{on} * R_{SEN} = Vin * R_{SEN} / L \tag{4}$$

$$M_2 = M_{off} * R_{SEN} = (Vout - Vin) * R_{SEN} / L \tag{5}$$

In Figure10, a small increase in the load current causes the sampled signal to increase by ΔVsamp0. The effect of this load change, ΔVsamp1, at the end of the first switching cycle is

$$\Delta V_{samp1} = -(\frac{M_2 - M_c}{M_1 + M_c}) * \Delta V_{samp0} \tag{6}$$

So, When No compensation ramp signal is added, which Mc is zero, then:

$$\Delta V_{samp1} = -(\frac{M_2}{M_1}) * \Delta V_{samp0} = -(\frac{D}{1-D}) * \Delta V_{samp0} \tag{7}$$

When D > 0.5, ΔVsamp1 will be greater than ΔVsamp0. In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase.

After a compensation ramp is added to the control signal. To ensure that the perturbed signal converges we must maintain:

$$\left| -(\frac{M_2 - M_c}{M_1 + M_c}) \right| < 1 \tag{8}$$

The compensation ramp has been added internally in the SCT81620. The slope of this compensation ramp has been selected to satisfy most applications, and it's value depends on the switching frequency. This slope can be calculated using the formula:

$$M_c = V_{SL} * F_s \tag{9}$$

VSL is the amplitude of the internal compensation ramp and FS is the controller's switching frequency.

For more flexibility, slope compensation can be increased by adding one external resistor, RSL, in the ISEN's path. Figure13 shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the SCT81620. When using external slope compensation, the formula for Mc becomes:

$$M_c = (V_{SL} + K * R_{SL}) * F_s \tag{10}$$

A typical value for factor K is 40 μA.

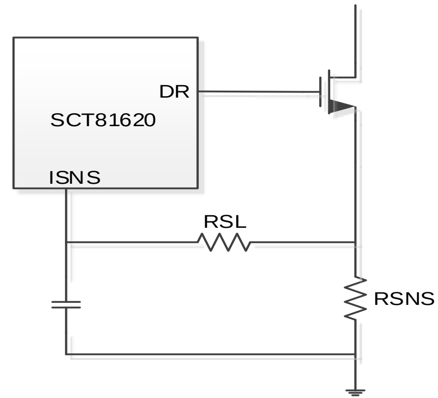


Figure13 .External RSL to increase slope compensation

Adjustable Peak Current Limit

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold. Peak inductor current limit (IPEAK-CL) in steady state is calculated as shown in:

$$I_{PEAK\_CL} = \frac{V_{SENSE} - 40uA \times R_{SL} \times D}{R_{SNS}} \quad (11)$$

Where

- V_{SENSE} is ISEN pin limiting voltage (Typ.=146.5mV)
- $I_{PEAK\text{-}CL}$ is the inductor peak current limit
- R_{SL} is Slope compensation resistor
- D is Duty cycle
- R_{SNS} is the Inductance peak current detection resistance

When overload happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high. When COMP voltage is clamped for 64 cycles, the controller stops working. After remaining OFF for 32768 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high， after soft start time and COMP still keep high for 64 cycles， the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

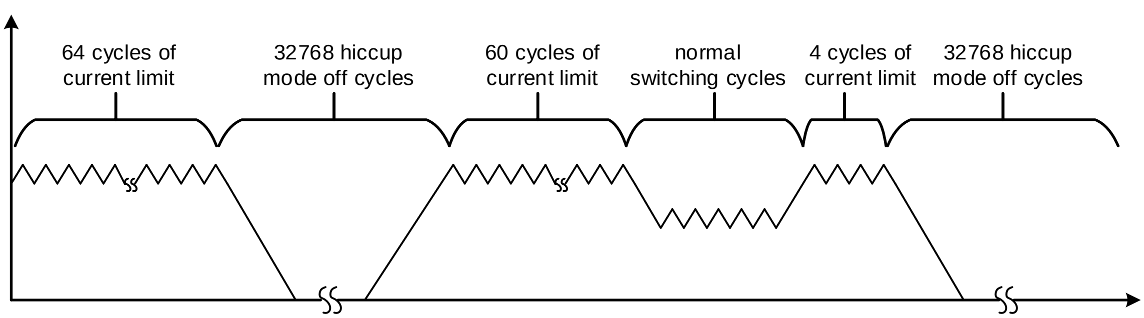


Figure14. Hiccup Mode Protection

Because D can be variable under different Vin, IPEAK-CL is not stable under different Vin when using external slope compensation resistor, so for an accurate peak current limit operation over the input supply voltage, SCT recommends using only the fixed slope compensation.

Output Voltage

The output voltage is set by an external resistor divider RFBT and RFBB in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of RFBT can be calculated by Equation 12.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{12}$$

where:

- V_{REF} is the feedback reference voltage, typical 1.26V

Frequency Adjust/Shutdown/ Synchronization

The switching frequency of the SCT81620 can be adjusted between 100 kHz and 2.2 MHz using a single external resistor. This resistor must be connected between the FA/SYNC/SD pin and ground, Equation 13 can be used to estimate the frequency adjust resistor.

$$\mathrm{R_{FA}}(\mathrm{k\Omega}) = \frac{19700}{fsw(kHz)} - 1.177 \tag{13}$$

The SCT81620 can also be synchronized to an external clock. The external clock must be connected between the FA/SYNC/SD pin and ground, as shown in Figure 16. The frequency adjust resistor may remain connected while synchronizing a signal, therefore if there is a loss of signal, the switching frequency will be set by the frequency adjust resistor.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal (>1.27V) appears on the FA/SYNC/SD pin over 30uS, the SCT81620 stops switching and goes into a low current mode. The total supply current of the IC reduces to 3.7 µA, typically, under these conditions.

Figure 17 and Figure 18 show an implementation of a shutdown function when operating in frequency adjust mode and synchronization mode, respectively. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground forces the clock to run at a certain frequency. Pulling this pin high shuts down the IC. In frequency adjust or synchronization mode, a high signal for more than 30 µs shuts down the IC.

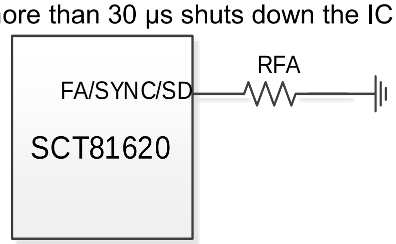


Figure15. Frequency Adjust

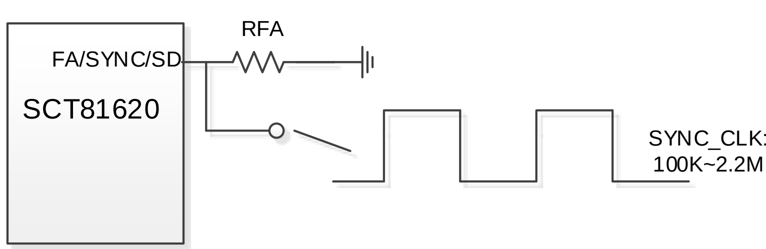


Figure16. Frequency Sync

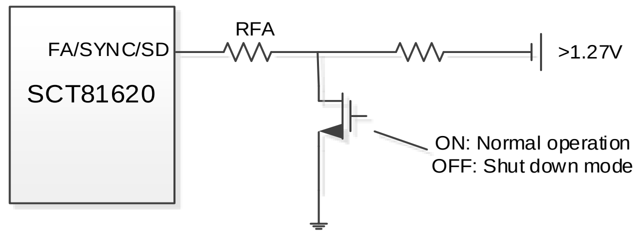


Figure17. Shutdown operation in Frequency Adjust Mode

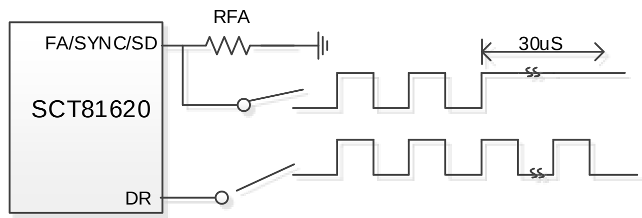


Figure18. Shutdown operation in Frequency Synchronization Mode

APPLICATION INFORMATION

Typical Application (Boost)

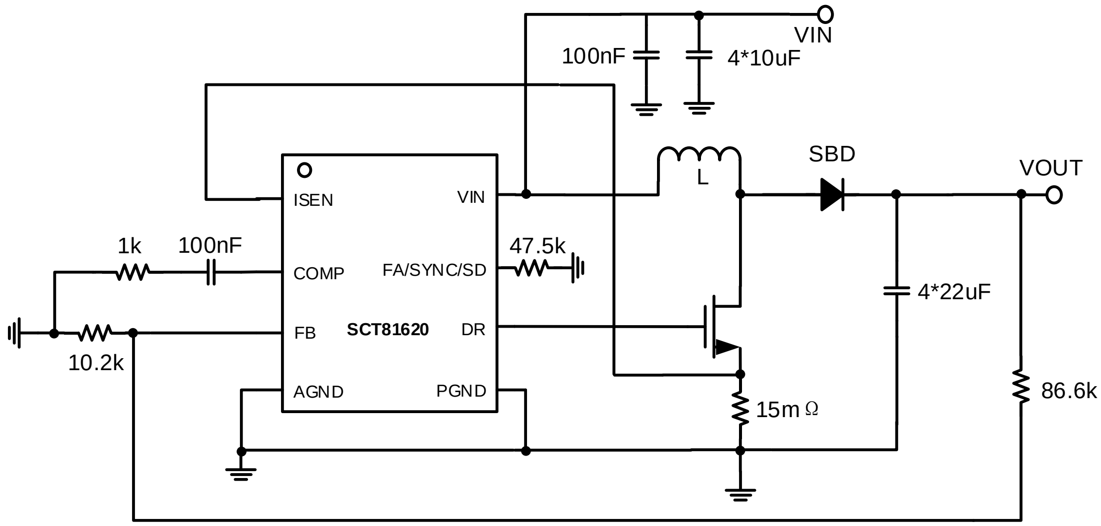


Figure 19. Application Schematic, 3V to 11V, 2A Boost Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 3V to 11V
Output Voltage	12V
Maximum Output Current	3A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Boost)

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±50% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boot converter, calculate the inductor DC current as in Equation 14

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{14}$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in Equation 15.

$$I_{LPP} = \frac{1}{L \times (\frac{1}{V_{OUT}-V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}} \tag{15}$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, ILPEAK, is calculated as in Equation 16

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \tag{16}$$

Set the current limit of the SCT81620 higher than the peak current ILPEAK and select the inductor with the saturation current higher than the current limit.

Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using Equation 17.

$$I_{CIN(RMS)} = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times L \times fsw} \tag{17}$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor should be chosen in the range of 10 μF to 40 μF. If a value lower than 10 μF is used, then problems with impedance interactions or switching noise can affect the SCT81620. To improve performance, especially with Vin below 8 volts, it is recommended to use a 2.2 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the VIN pin with only a bypass capacitor attached to the VIN pin directly. A 0.1-μF or 1-μF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, 3～4x 22μF ceramic output capacitors work for most applications. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the switch node. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 18 and 19 to calculate the minimum required effective capacitance, C_{OUT}.

$$V_{ripple\_C} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (18)$$

$$V_{ripple\_ESR} = I_{Lpeak} \times ESR \quad (19)$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance RDS_ON, the minimum gate threshold voltage VTH_MIN, the total gate charge Qg, the reverse transfer capacitance CRSS, and the maximum drain to source voltage VQ_MAX. The peak switching voltage between drain to source in a Boost is given by

$$V_{SW\_PEAK} = V_{IN} + V_D \quad (20)$$

Then the VQ_MAX of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q\_PEAK} = I_{LPEAK} \quad (21)$$

The RMS current through the MOSFET is calculated by:

$$I_{Q\_RMS} = \sqrt{(I_{LDC}{}^2 + \frac{I_{LPP}}{12}) * D} \quad (22)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + \left(V_O + V_{IN\_MIN}\right) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (23)$$

Where

I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using Equation 24.

$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \tag{24}$$

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

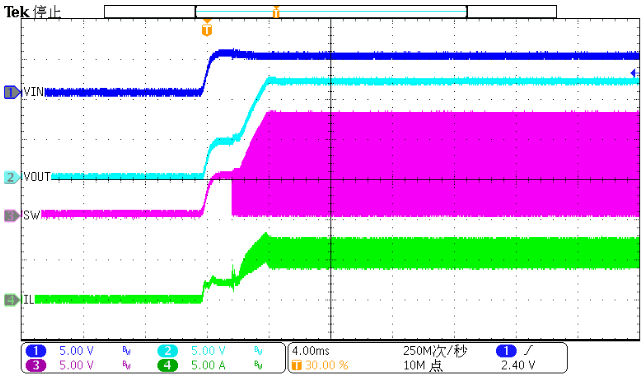


Figure 20. Power up(Iload=2A)

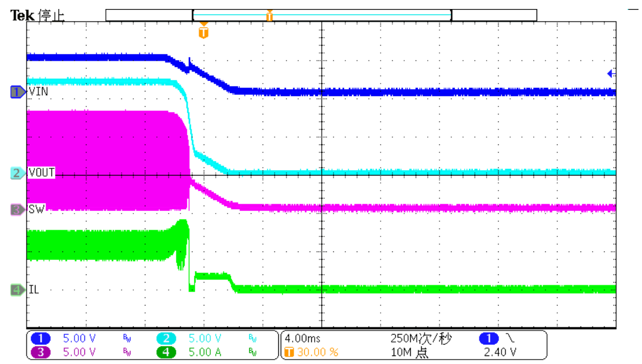


Figure 21. Power down(Iload=2A)

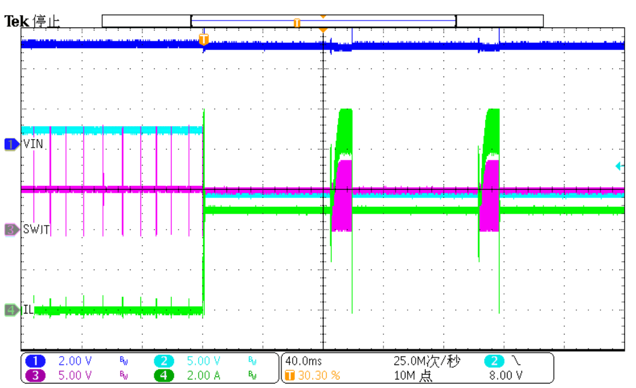


Figure 22. Over current protection (Iload=5A)

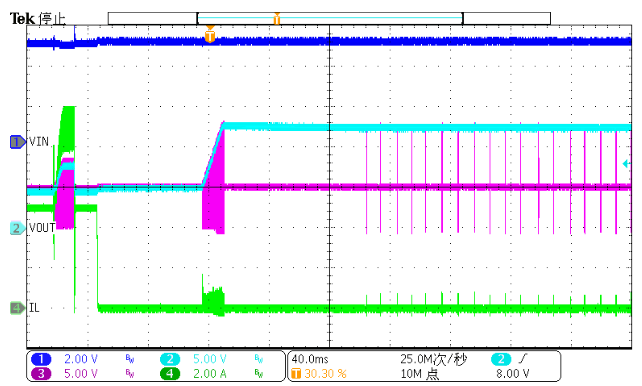


Figure 23. Over current recovery (Iload=5A)

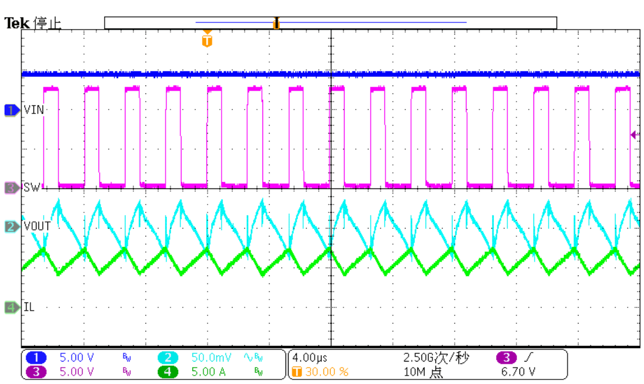


Figure 24. Steady-state (Iload=2A)

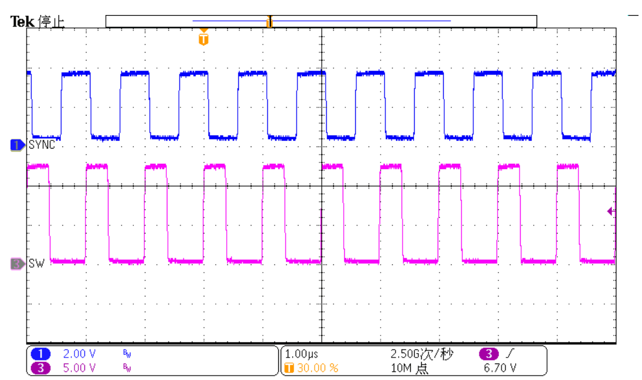


Figure 25. Sync Frequency

Typical Application (Sepic)

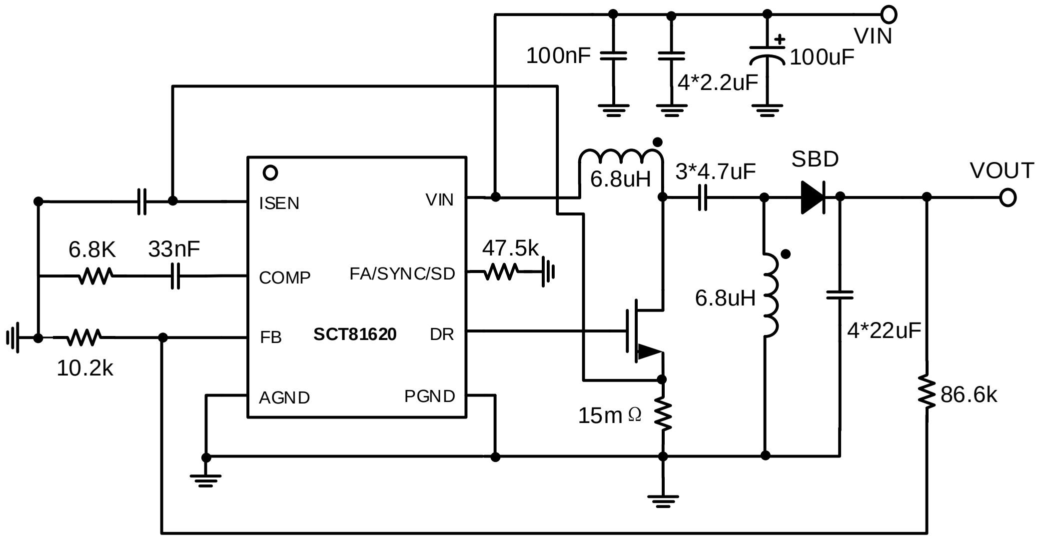


Figure 26. Application Schematic, 5V to 50V, 2A Sepic Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Sepic)

A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20% to 40% of the maximum input current at the minimum input voltage. The current ripple flowing in inductors L1 and L2 is given by:

$$\Delta I_{L1} = I_{IN} \times 40\% = I_O \times \frac{V_O}{V_{IN\_MIN}} \times 40\% \tag{25}$$

$$\Delta I_{L2} = I_O \times 40\% = I_O \times 40\% \tag{26}$$

Normally we can select equal value for the inductors L1 and L2, derived as:

$$L_1 = L_2 = L = \frac{V_{IN\_MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \tag{27}$$

Where

- f_{SW} is the switching frequency.

Note that the saturation current of inductors should be greater than peak current flowing in inductors, given by:

$$I_{L1\_PEAK} = I_{IN} + \frac{\Delta I_L}{2} = I_O \times \frac{V_O}{V_{IN\_MIN}} \times (1 + \frac{40\%}{2}) \tag{28}$$

$$I_{L2\_PEAK} = I_O + \frac{\Delta I_L}{2} = I_O \times (1 + \frac{40\%}{2}) \tag{29}$$

If L1 and L2 are wound in same core as a coupled inductor, the inductance required will be half due to the mutual induction, calculated by:

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN\_MIN}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX} \tag{30}$$

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance RDS_ON, the minimum gate threshold voltage VTH_MIN, the total gate charge Qg, the reverse transfer capacitance CRSS, and the maximum drain to source voltage VQ_MAX. The peak switching voltage between drain to source in a SEPIC is given by:

$$V_{SW\_PEAK} = V_{IN} + V_O + V_D \tag{31}$$

Then the V_{Q_MAX} of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q\_PEAK} = I_{L1\_PEAK} + I_{L2\_PEAK} \tag{32}$$

The RMS current through the MOSFET is calculated by:

$$I_{Q\_RMS} = I_O \times \sqrt{\frac{\left(V_O + V_{IN\_MIN} + V_D\right) \times \left(V_O + V_D\right)}{V_{IN\_MIN}^2}} \tag{33}$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + \left(V_O + V_{IN\_MIN}\right) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \tag{34}$$

Where

- *I_G is the gate drive current.*

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D\_PEAK} = V_{IN\_MAX} + V_{O\_MAX} \tag{35}$$

The diode should also be capable to flow switch peak current IQ_PEAK.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \tag{36}$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$I_{CS\_RMS} = I_O \times \sqrt{\frac{V_O + V_D}{V_{IN\_MIN}}} \tag{37}$$

There is a large RMS current through coupling capacitor relative to output power. Ensure the coupling capacitor can withstand it with good heat generation to have proper thermal performance.

Input Capacitor Selection

The SEPIC has an inductor at input side thus the input current is continuous and triangular. The RMS current flowing through the input capacitor is given by:

$$I_{IN\_RMS} = \frac{\Delta I_{L1}}{\sqrt{12}} \tag{38}$$

Since input current ripple is relative low, the capacitance would be not too critical. While 100μF in total or higher value is strongly recommended in order to provide stable input supply.

Output Capacitor Selection

Similar to boost converter, the SEPIC output capacitor suffers large current ripple. The capacitance must be enough to provide the load current. The maximum voltage ripple in the output capacitor is:

$$\Delta V_{OUT} = \frac{I_O \times D_{MAX}}{C_{OUT} \times f_{SW}} + ESR \times \left(I_{L1\_PEAK} + I_{L2\_PEAK}\right) \tag{39}$$

Assuming ceramic capacitors are used here and ESR can be ignored, the output capacitor is given by:

$$C_{OUT} \geq \frac{I_O \times D_{MAX}}{\Delta V_{OUT} \times f_{SW}} \tag{40}$$

The output capacitor must have a enough RMS current rating to handle the maximum RMS current in the output capacitor, calculated by:

$$I_{COUT\_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \qquad (41)$$

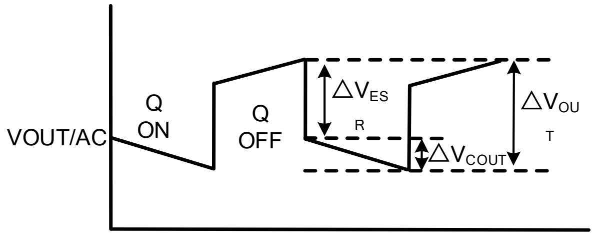


Figure 27. Output Voltage Ripple

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

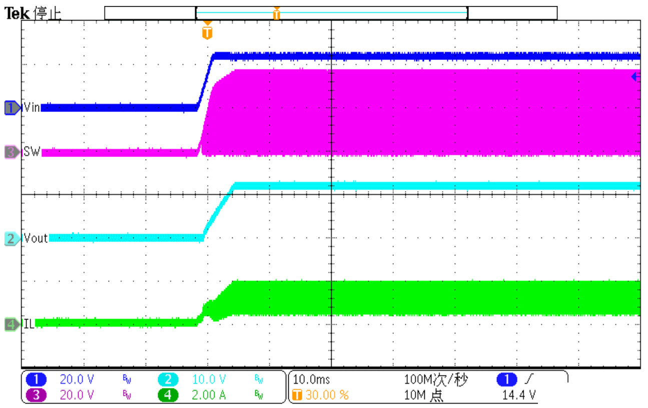


Figure 28. Power up(Iload=2A)

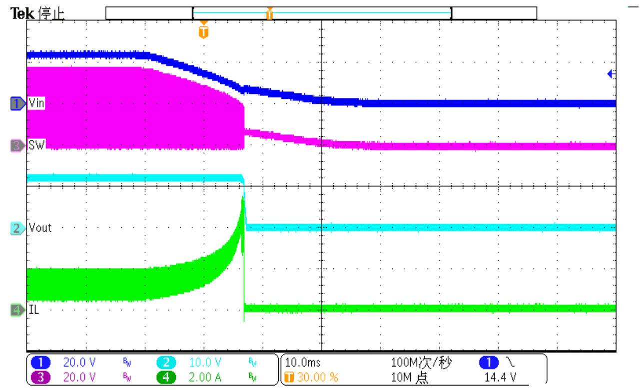


Figure 29. Power down(Iload=2A)

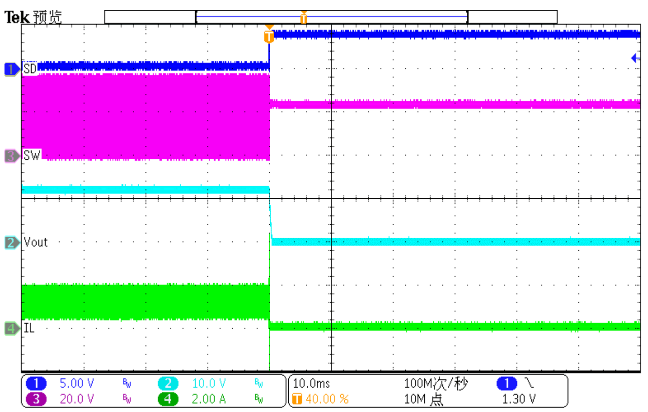


Figure 30. Shutdown remove

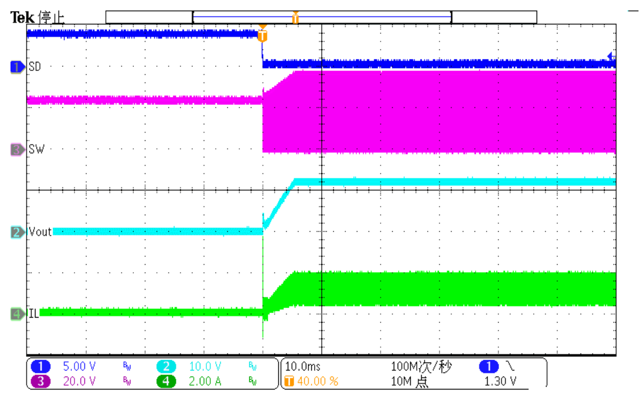


Figure 31. Shutdown remove

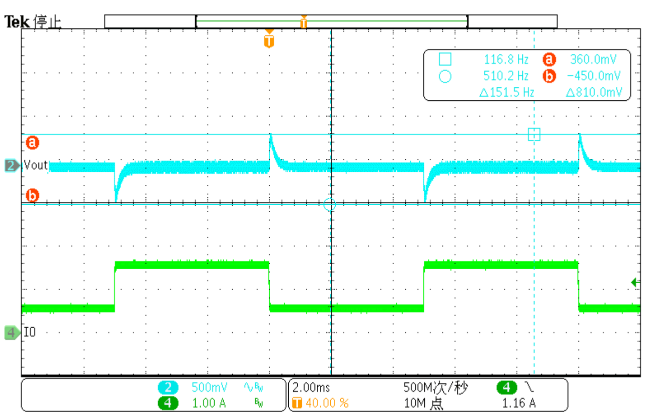


Figure 32. LoadTrans (Iload=0.5A-1.5A)

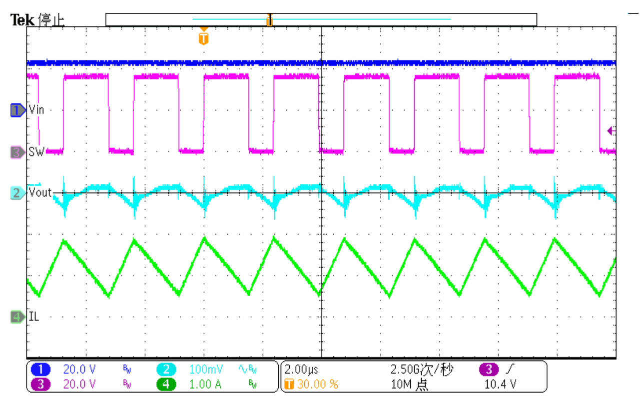


Figure 33. steady-state (Iload=2A)

Layout Guideline

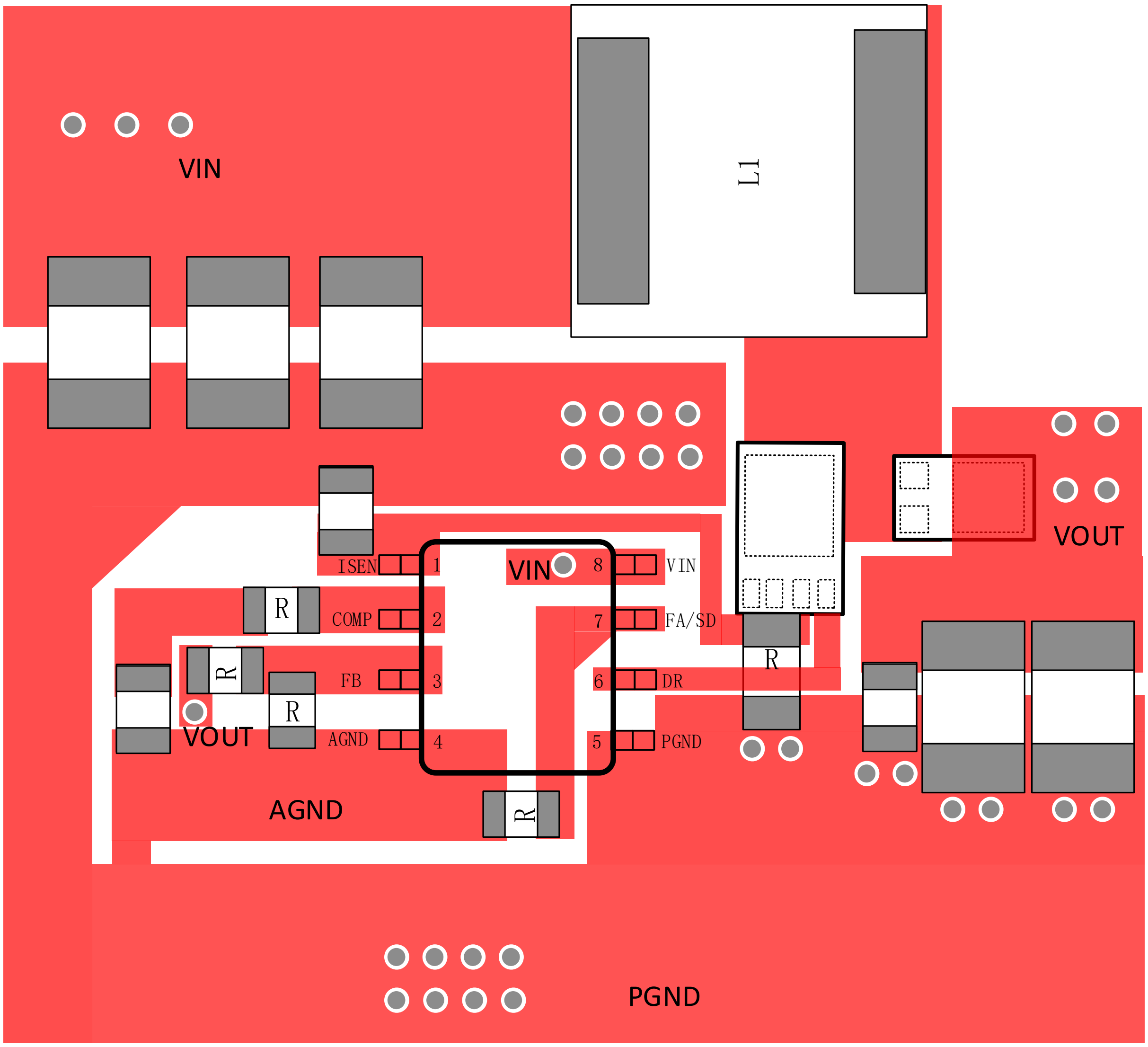
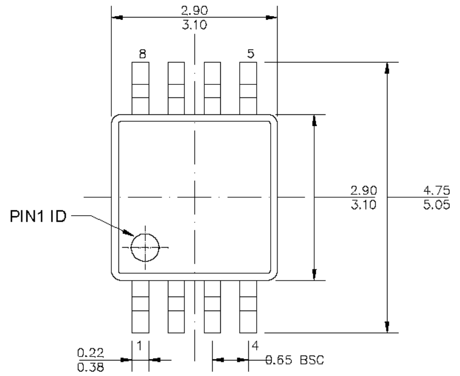
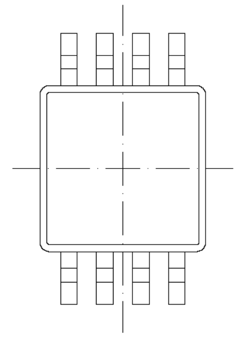


Figure 34. BOOST PCB Layout

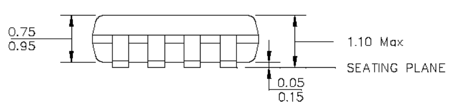
PACKAGE INFORMATION



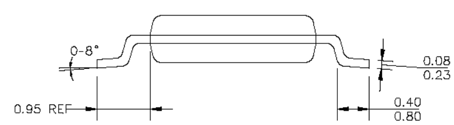
TOP VIEW



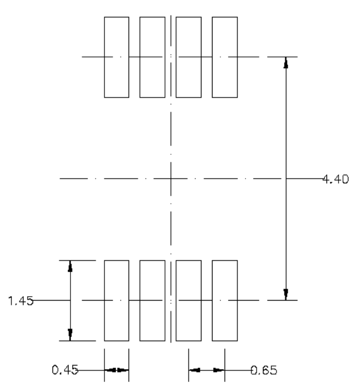
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

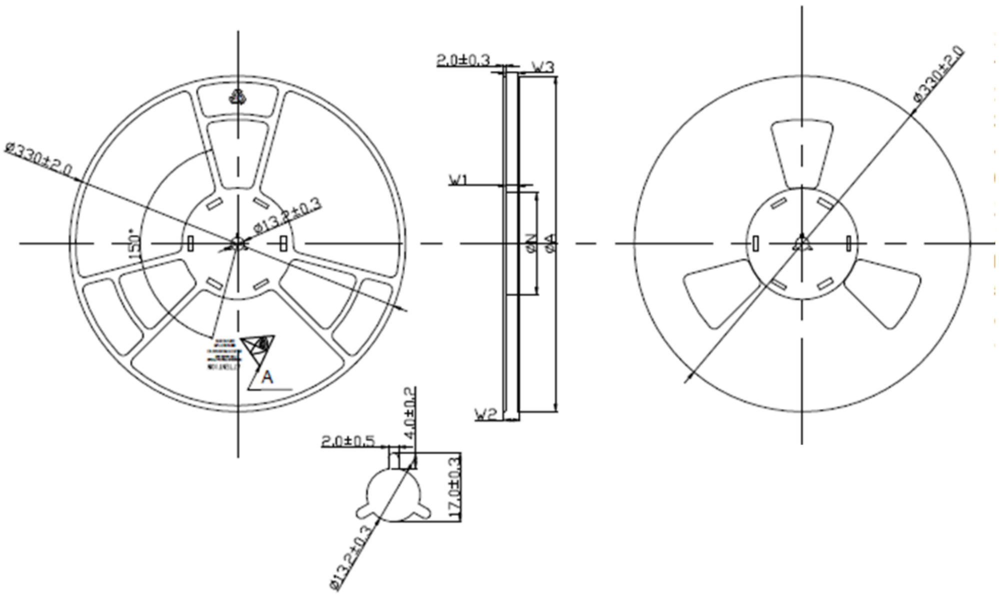


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) DRAWING MEETS JEDEC MO-187, VARIATION BA.
4) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS					
TYPE WIDTH	ØA	ØN	W1(+2/0)	W2(Max)	W3(Max)
12MM	330±2.0	100±1.0	12.4	18.4	11.9/15.4